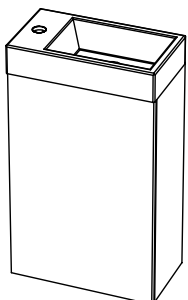
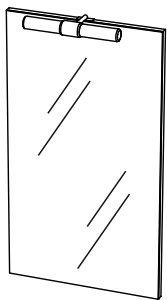
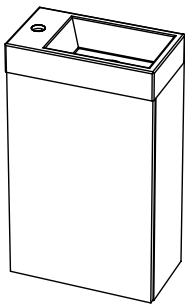
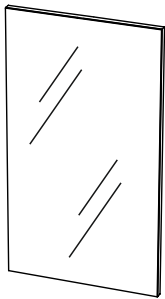
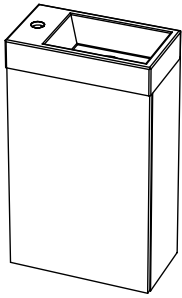
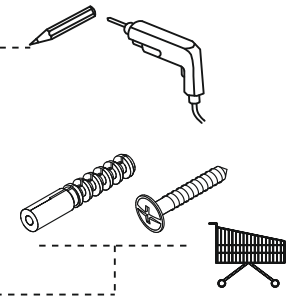
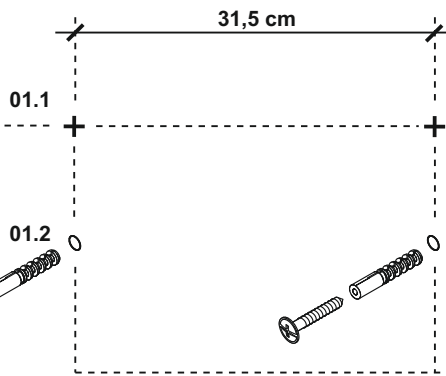
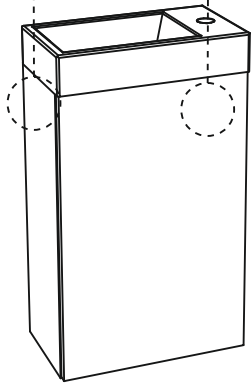


1D



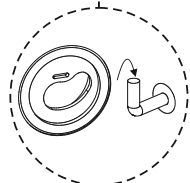
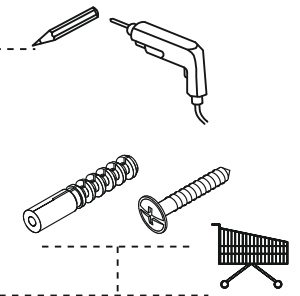
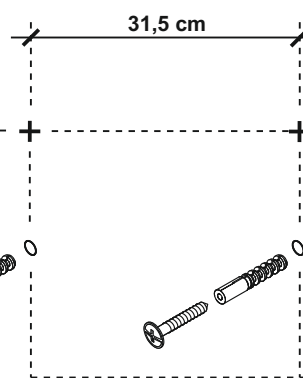
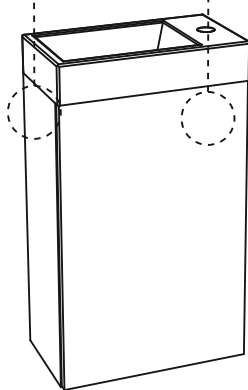
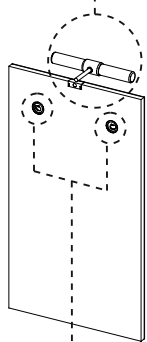
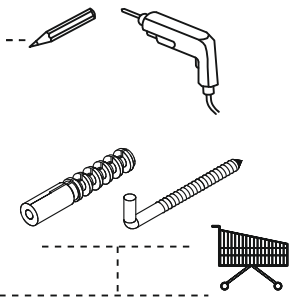
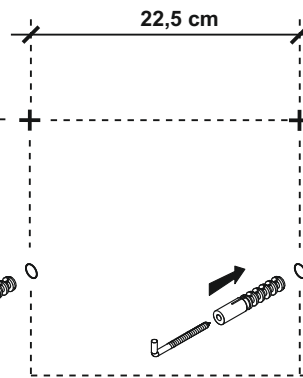
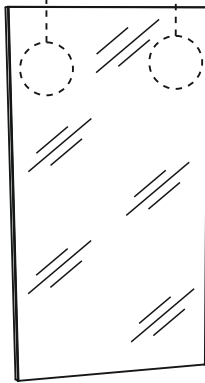
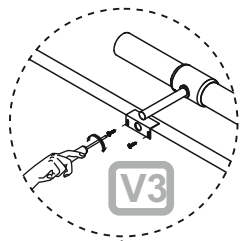
1a

V1



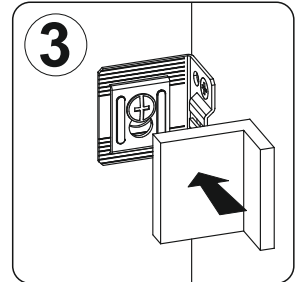
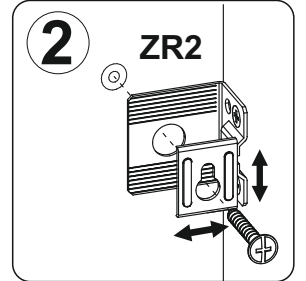
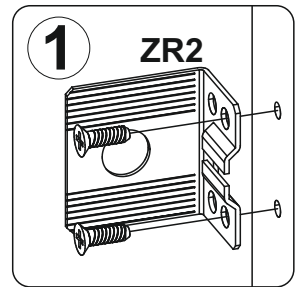
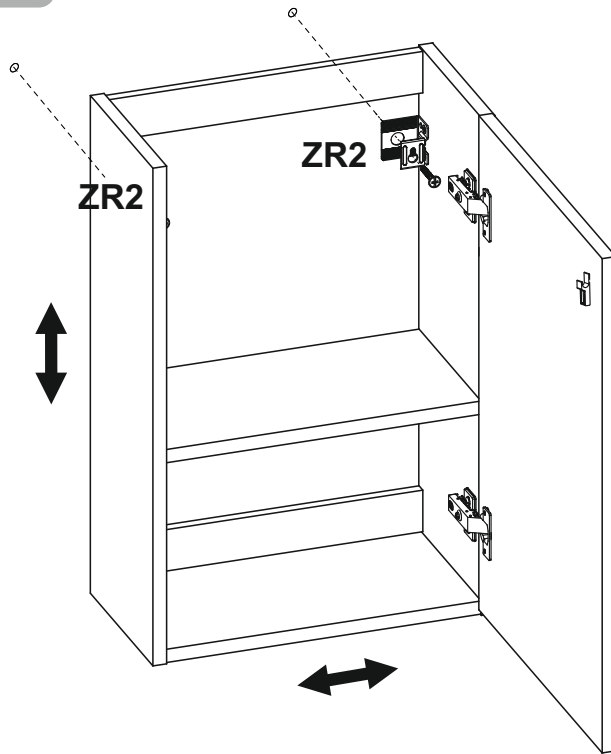
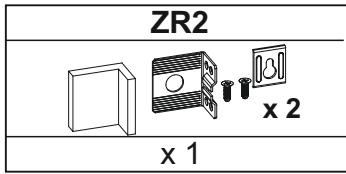
1b

V2 V3



1c

V1 V2 V3



2

V1 V2 V3



03.

04.



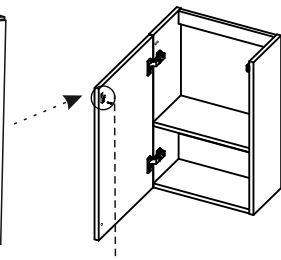
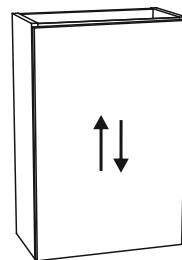
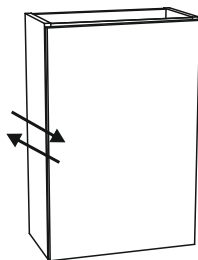
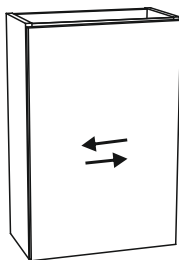
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03.

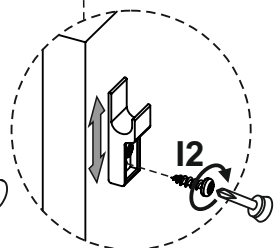
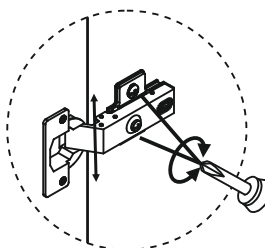
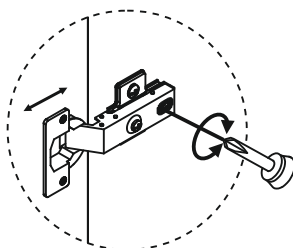
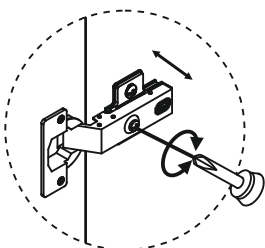
04.

3

V1 V2 V3

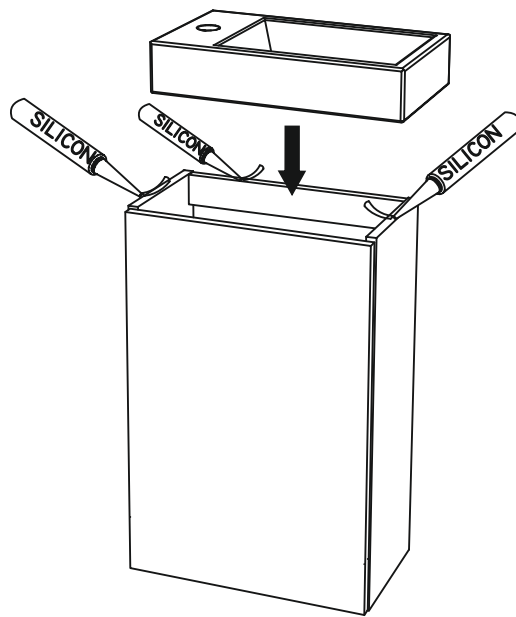


I2

UP3x12
x 1



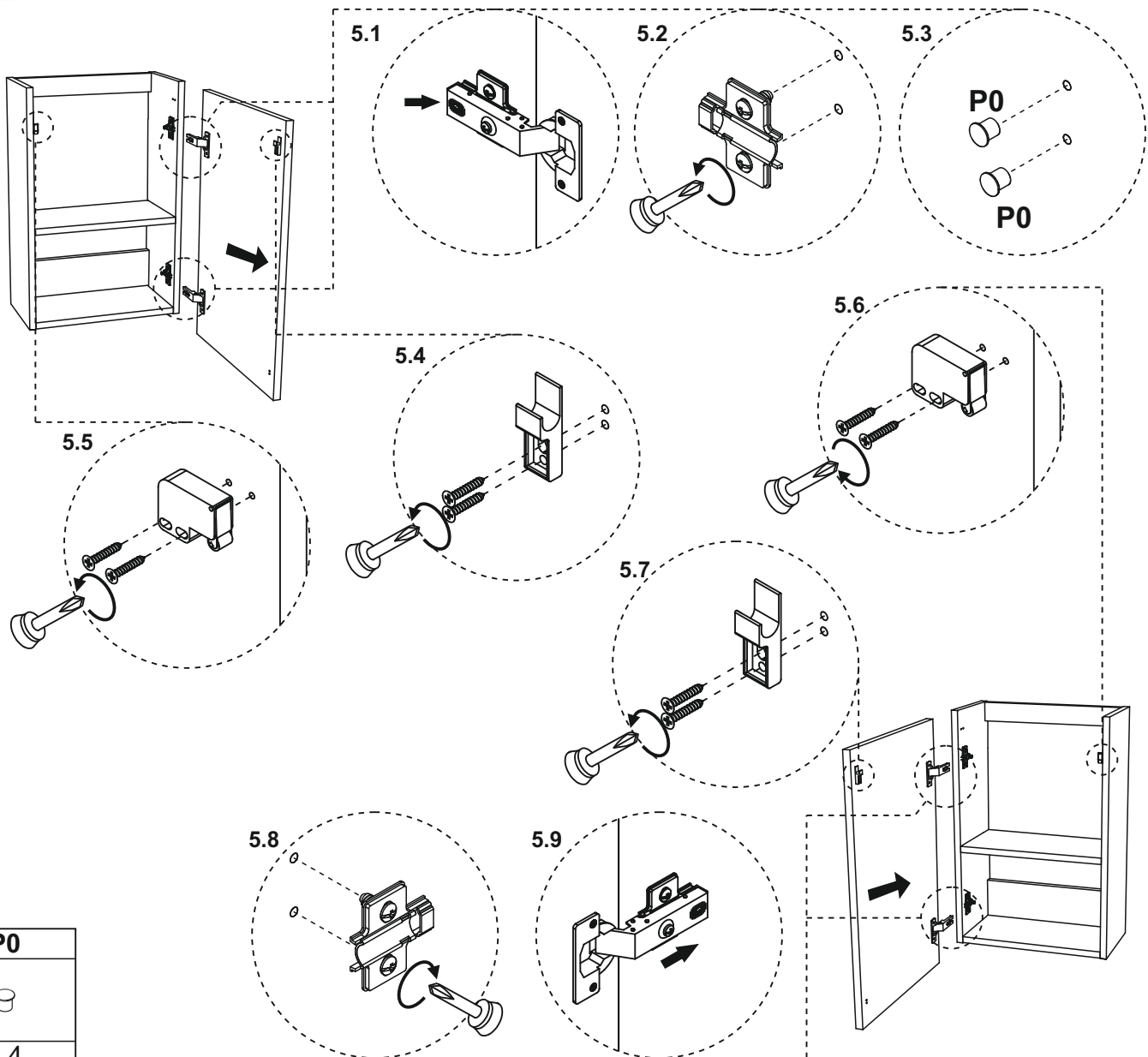
4


V1 V2 V3



5

V1 V2 V3



P0

x 4